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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 10/758,539  | 01/16/2004  | Gyung-su Byon        | SEC.1129            | 5592             |
| 20987   | 7590        | 07/27/2005           | EXAMINER            |                  |
| VOLENTINE FRANCOS, & WHITT PLLC<br>ONE FREEDOM SQUARE<br>11951 FREEDOM DRIVE SUITE 1260<br>RESTON, VA 20190 |             |                      | LE, THONG QUOC      |                  |
|   |             |                      | ART UNIT            | PAPER NUMBER     |
|   |             |                      | 2827                |                  |

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                        |                     |  |
|------------------------------|------------------------|---------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b> | <b>Applicant(s)</b> |  |
|                              | 10/758,539             | BYON, GYUNG-SU      |  |
|                              | <b>Examiner</b>        | <b>Art Unit</b>     |  |
|                              | Thong Q. Le            | 2827                |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-13 is/are allowed.
- 6) ☒ Claim(s) 1 and 6-8 is/are rejected.
- 7) ☒ Claim(s) 2-5 and 9 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>0405</u> | 6) <input type="checkbox"/> Other: ____  |

**DETAILED ACTION**

1. Claims 1-13 are presented for examination.

***Information Disclosure Statement***

2. This office acknowledges receipt of the following items from the Applicant:  
Information Disclosure Statement (IDS) filed on 04/06/2005.
3. Information disclosed and list on PTO 1449 was considered.

***Priority***

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1,6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U.S. Patent No. 5,614,855).

Regarding claims 1, 6-8, Lee et al. disclose a semiconductor device (Figure 2), comprising:

a duty cycle correction (DCC) circuit (140) that receives first and second clock signals (reference clock input) and outputs a duty cycle adjusted clock signal (Clock

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output); and a control circuit (160) that detects a process variation and controls respective slew rates of the first and second clock signals based on the detected process variation (ABSTRACT, Column 13, lines 43-64), and an amplifying circuit that receive an external clock signal and outputs the first and second clock signals corresponding to the external clock (Figure 2, 100).

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1,6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu et al. (U.S. Patent No. 6,643,790).

Regarding claims 1, 6-8, Yu et al. disclose a semiconductor device (Figure 1), comprising:

a duty cycle correction (DCC) circuit (ABSTRACT) that receives first and second clock signals (Figure 1, ICLK, /ICLK) and outputs a duty cycle adjusted clock signal (OCLK, /OCLK); and a control circuit (Column 7, lines 45-54) that detects a process variation and controls respective slew rates of the first and second clock signals based on the detected process variation (Column 3, lines 10-30), and an amplifying circuit that

receive an external clock signal and outputs the first and second clock signals corresponding to the external clock (Figure 2A, Column 7, lines 55-59).

***Allowable Subject Matter***

8. Claims 2-5,9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-5,9 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Lee et al. (U.S. Patent No. 5,614,855), Yu et al. (U.S. Patent No. 6,643,790), and others, does not teach the claimed invention having a DCC circuit comprises a first inverter having an input that receives the first clock signal, and a second inverter having an input that receives the second clock signal and a third inverter having an input commonly connected to outputs of the first and second inverters, and a first variable capacitor connected between the input of the first inverter and a ground voltage; and a second variable capacitor connected between the input of the first inverter and the ground voltage, wherein respective capacitance values of the first and second variable capacitors are set by the control circuit.

9. Claims 10-13 are allowed.

Claims 10-13 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Lee et al. (U.S. Patent No. 5,614,855), and others, does not teach

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the claimed invention having a synchronous semiconductor memory device comprising: a first inverter having an input that receives a first clock signal, a second inverter having an input that receives a second clock signal which is opposite in phase to the first clock signal, a third inverter having an input commonly connected to outputs of the first and second inverters; a first capacitor unit having a plurality of capacitors that are selectively connected between the input of the first inverter and a ground voltage to define a first capacitance value between the first inverter and the ground voltage, a second capacitor unit having a plurality of capacitors that are selectively connected between the input of the second inverter and the ground voltage to define a second capacitance value between the second inverter and a control circuit that detects a process variation and controls respective slew rates of the first and second clock signals based on the detected process variation, wherein the control circuit controls the respective slew rates of the first and second clock signals by adjusting the first and second capacitance values of the first and second capacitor units, respectively.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le  
Primary Examiner  
Art Unit 2827

**THONG LEI  
PRIMARY EXAMINER**